4.2 One Byte Memory Modules

4.2.1 – 22 PIN SIP/SIMM DRAM MODULE

CAPACITY—64K, 256K WORDS OF 4 BITS
CONFIGURATION—SINGLE SIDED MODULE USING 64K OR 256K DEVICES
PACKAGE—22 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2–1

– 24 PIN SIP/SIMM DRAM MODULE

CAPACITY—128K, 512K WORDS OF 4 BITS
CONFIGURATION—DOUBLE SIDED MODULE USING 64K OR 256K DEVICES
PACKAGE—24 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2–1

– 30 PIN SIP/SIMM DRAM MODULE

CAPACITY—64K, 256K, 1M, 4M WORDS OF 8 OR 9 BITS, & 16M WORDS OF 8 BITS
CONFIGURATION—SINGLE SIDED MODULE
—USING 64K, 256K, 1M, 4M, OR 16M MEMORY DEVICES
LOGIC FEATURES—Some of the modules contain a “presence detect” feature which conists of outputs that supply an encoded value which defines the storage capacity of the module.
PACKAGE—30 PIN SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2–1

4.2.2 – 30 PIN SIP/SIMM DRAM MODULE FAMILY

CAPACITY —64K TO 8M WORDS OF 4 OR 5 BITS
—128K TO 16M WORDS OF 2 BITS
—256K TO 32M WORDS OF 1 BIT
CONFIGURATION—ONE OR TWO SIDED,
—USING 64K, 256K, 1M, OR 4M DEVICES
CAPACITY—32K, 64K, 128K, 256K WORDS OF 8 BITS
PACKAGE—30 PIN SIP MODULE
PIN ASSIGNMENT Fig. 4.2–2

4.2.3 – 23/25/26/28 PIN ZIP/SIMM DRAM MODULE FAMILY

CAPACITY —256K TO 16M WORDS OF 4 BIT
—1M TO 64M WORDS OF 1 BIT
CONFIGURATION—DOUBLE SIDED, USING 1M, 4M, 16M, OR 64M DEVICES
PACKAGE—THE X4 MODULES, 26 PIN ZIP/SIP MODULE
THE X1 MODULES, 23 PIN ZIP/SIP MODULE
PIN ASSIGNMENTS—Fig. 4.2–3
NOTE: At the highest density using 64M memory devices, the modules must be expanded to 25 or 28 pins to provide the needed addresses. These modules will be defined in more detail when the packages for the 64M memory devices have been defined.

4.2.4 – 60 PIN ZIP/SIMM SRAM MODULE

CAPACITY—2 X 64K, 2 X 256K, 2 X 1M WORDS OF 4 BITS
CONFIGURATION—DUAL BANK MODULE USING DEVICES WITH 64K, 256K, OR 1M WORDS—SELECTABLE AS 64K, 256K, OR 1M BY 8, 128K, 512K, OR 2M BY 4
PACKAGE—60 PIN SIP MODULE WITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4.2–4

– 70 PIN ZIP/SIMM SRAM MODULE

CAPACITY—64K, 256K, 1M WORDS OF 9 BITS
CONFIGURATION—SINGLE BANK MODULE USING DEVICES WITH 64K, 256K, OR 1M WORDS—SELECTABLE AS 64K, 256K, OR 1M BY 9
LOGIC FEATURE—SEPARATELY CONTROLLABLE BIT FOR USE AS PARITY BIT
PACKAGE—70 PIN SIP MODULE WITH ZIP TERMINAL CONFIGURATION
PIN ASSIGNMENTS—Fig. 4.2–5

PHYSICAL CONFIGURATION	4 DEVICES LONG				8 OR 9 DEVICES LONG			
	SINGLE BANK		DOUBLE BANK		SINGLE BANK			DOUBLE BANK
VERSION	N X 4	@ 4N X 1	2N X 4	N X 8	* N X 8(9)	* N X 8(9)	16M X 8	* 2N X 8(9)
1	$ A8	VSS	** NC	% NC	VDD	VDD	VDD	VDD
2	VDD	VDD	A8	A8	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
3	D0	$\overline{RE0}$	VDD	VDD	DQ0	DQ0	DQ0	DQ0
4	Q0	Q	D0	DQ0	A0	A0	A0	A0
5	$\overline{CE}$	A3	Q0	DQ1	A1	A1	A1	A1
6	A7	A6	$\overline{CE}$	$\overline{CE}$	DQ1	DQ1	DQ1	DQ1
7	A5	D	A7	A7	A2	A2	A2	A2
8	A4	$\overline{W}$	A5	A5	A3	A3	A3	A3
9	D1	$\overline{RE1}$	A4	A4	VSS	VSS	VSS	VSS
10	Q1	A0	D1	DQ2	DQ2	DQ2	DQ2	DQ2
11	$\overline{W}$	A7	Q1	DQ3	A4	A4	A4	A4
12	A1	A8	$\overline{W}$	$\overline{W}$	A5	A5	A5	A5
13	A3	$\overline{CE}$	A1	A1	DQ3	DQ3	DQ3	DQ3
14	A6	$\overline{RE2}$	A3	A3	A6	A6	A6	A6
15	Q2	A2	A6	A6	A7	A7	A7	A7
16	D3	A1	Q2	DQ4	DQ4	DQ4	DQ4	DQ4
17	A2	@ A9	D2	DQ5	A8	A8	A8	A8
18	A0	A4	A2	A2	* A9	* A9	A9	* A9
19	$\overline{RE}$	$\overline{RE3}$	A0	A0	* A10	NC	A10	$\overline{RE2}$
20	D3	A5	RE1	$\overline{RE}$	DQ5	DQ5	DQ5	DQ5
21	Q0	VDD	D3	DQ6	$\overline{W}$	$\overline{W}$	$\overline{W}$	$\overline{W}$
22	VSS	VSS	Q3	DQ7	VSS	VSS	VSS	VSS
23			VSS	VSS	DQ6	DQ6	DQ6	DQ6
24			*** $\overline{RE2}$	NC	# NC	PD1	A11	PD1
25					DQ7	DQ7	DQ7	DQ7
26					Q8	PD2	NC	PD2
27					$\overline{RE}$	$\overline{RE}$	$\overline{RE}$	$\overline{RE1}$
28					$\overline{CE8}$	NC	NC	NC
29					D8	DQ8	NC	DQ8
30					VDD	VDD	VDD	VDD

TOP VIEW

* ON THE 30 PIN MODULE, 1M & 4M DEVICES MAY BE USED. PINS 18 & 19 ARE USED TO PROVIDE ADDRESS EXPANSION. THE OTHER MODULES WILL ACCOMIDATE 64K & 256K DEVICES ONLY.

** OPTIONAL VSS

*** NC FOR SINGLE BANK VERSION

$ OPTIONAL VSS WHEN A8 NOT NEEDED

OPTIONAL REFRESH (F) FUNCTION

@ ON THE 22 PIN 4N X 1 MODULE, 1 MB & 4 MB DEVICES MAY BE USED. PIN 17 IS USED FOR ADDRESS EXPANSION

% POTENTIAL VSS

PRESENCE DETECT TRUTH TABLE

SIZE	256K	512K	1M
PIN			
PD1	L	H	L
PD2	H	L	L

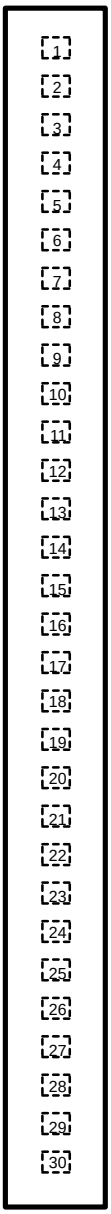
CONFIGURATION DEFINES THE PHYSICAL ARRANGEMENTS OF THE MEMORY DEVICES ON THE MODULE, GIVING LENGTH AND NUMBER OF SIDES POPULATED.

VERSION IS THE LOGIC ORGANIZATION OF THE MODULE WHERE ”N” IS THE CAPACITY OF THE MEMORY DEVICE USED.

FIGURE 4.2–1

22, 24,& 30 PIN DRAM MODULES

PHYSICAL CONFIGURATION	4 OR 5 DEVICES LONG SINGLE SIDED			4 OR 5 DEVICES LONG DOUBLE SIDED		
VERSION	**N X 4(5)**	**2N X 2**	**4N X 1**	**2N X 4(5)**	**4N X 2**	**8N X 1**
1	VDD					
2	D4	NC	NC	D4	NC	NC
3	Q4	NC	NC	Q4	NC	NC
4	A8					
5	A9					
6	*A10					
7	D3	D1	NC	D3	D1	NC
8	Q3	Q1	NC	Q3	Q1	NC
9	VSS					
10	A6					
11	A7					
12	A2					
13	A1					
14	D2	NC	D	D2	NC	D
15	Q2	NC	Q	Q2	NC	Q
16	A4					
17	A5					
18	A3					
19	A0					
20	D1	D0	NC	D1	D0	NC
21	Q1	Q0	NC	Q1	Q0	NC
22	VSS					
23	$\overline{W}$					
24	$\overline{CE}$	$\overline{CE1}$				
25	NC	$\overline{CE2}$				
26	$\overline{RE}$			$\overline{RE1}$		
27	NC	NC	NC	$\overline{RE2}$		
28	D0	NC	$\overline{CE3}$	D0	NC	$\overline{CE3}$
29	Q0	NC	$\overline{CE4}$	Q0	NC	$\overline{CE4}$
30	VDD					



30 PIN SIP MODULE TOP VIEW

* PIN 6 RESERVED FOR OPTIONAL REFRESH (F) WHEN NOT NEEDED FOR A10

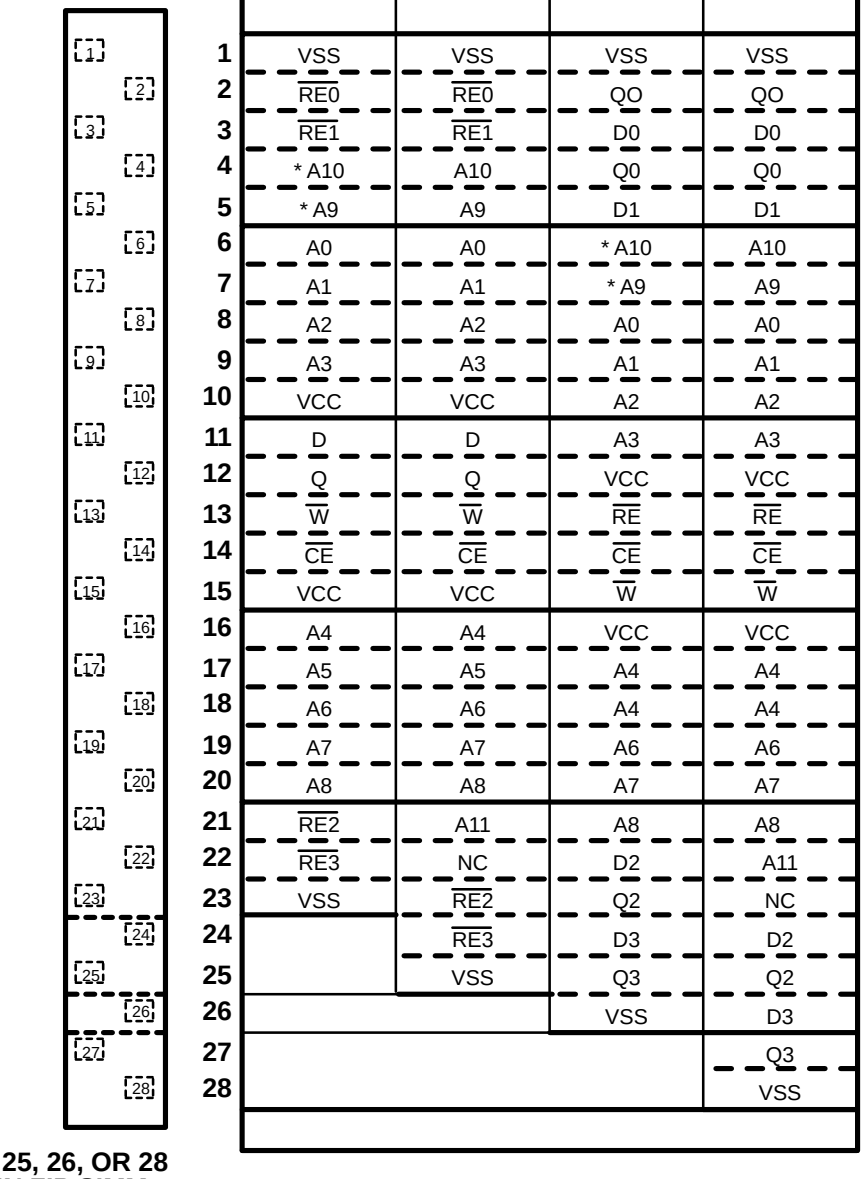
CONFIGURATION DEFINES THE PHYSICAL ARRANGEMENTS OF THE MEMORY DEFICES ON THE MODULE, GIVING LENGTH AND NUMBER OF SIDES POPULATED

VERSION IS THE LOGIC ORGANIZATION OF THE MODULE WHERE "N" IS THE CAPACITY OF THE MEMORY DEVICE USED

MEMORY DEVICES WITH A CAPACITY OF UP TO 4Mb BY 1 CAN BE ACCOMIDATED ON THE MODULES DEFINED IN THIS STANDARD

FIGURE 4.2–2

30 PIN DRAM MODULE FAMILY



VERSION	@ N X 1	# N X 1	& N X 4	% N X 4
1	VSS	VSS	VSS	VSS
2	$\overline{RE0}$	$\overline{RE0}$	QO	QO
3	$\overline{RE1}$	$\overline{RE1}$	D0	D0
4	* A10	A10	Q0	Q0
5	* A9	A9	D1	D1
6	A0	A0	* A10	A10
7	A1	A1	* A9	A9
8	A2	A2	A0	A0
9	A3	A3	A1	A1
10	VCC	VCC	A2	A2
11	D	D	A3	A3
12	Q	Q	VCC	VCC
13	$\overline{W}$	$\overline{W}$	$\overline{RE}$	$\overline{RE}$
14	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
15	VCC	VCC	$\overline{W}$	$\overline{W}$
16	A4	A4	VCC	VCC
17	A5	A5	A4	A4
18	A6	A6	A4	A4
19	A7	A7	A6	A6
20	A8	A8	A7	A7
21	$\overline{RE2}$	A11	A8	A8
22	$\overline{RE3}$	NC	D2	A11
23	VSS	$\overline{RE2}$	Q2	NC
24		$\overline{RE3}$	D3	D2
25		VSS	Q3	Q2
26			VSS	D3
27				Q3
28				VSS

23, 25, 26, OR 28 PIN ZIP SIMM TOP VIEW

N = THE ADDRESS CAPACITY OF THE MEMORY DEVICE USED

@ THIS CONFIGURATION IS APPLICABLE TO 1M, 4M, & 16M X 1 DEVICES.

THIS CONFIGURATION IS APPLICABLE TO A 64M X 1 DEVICE

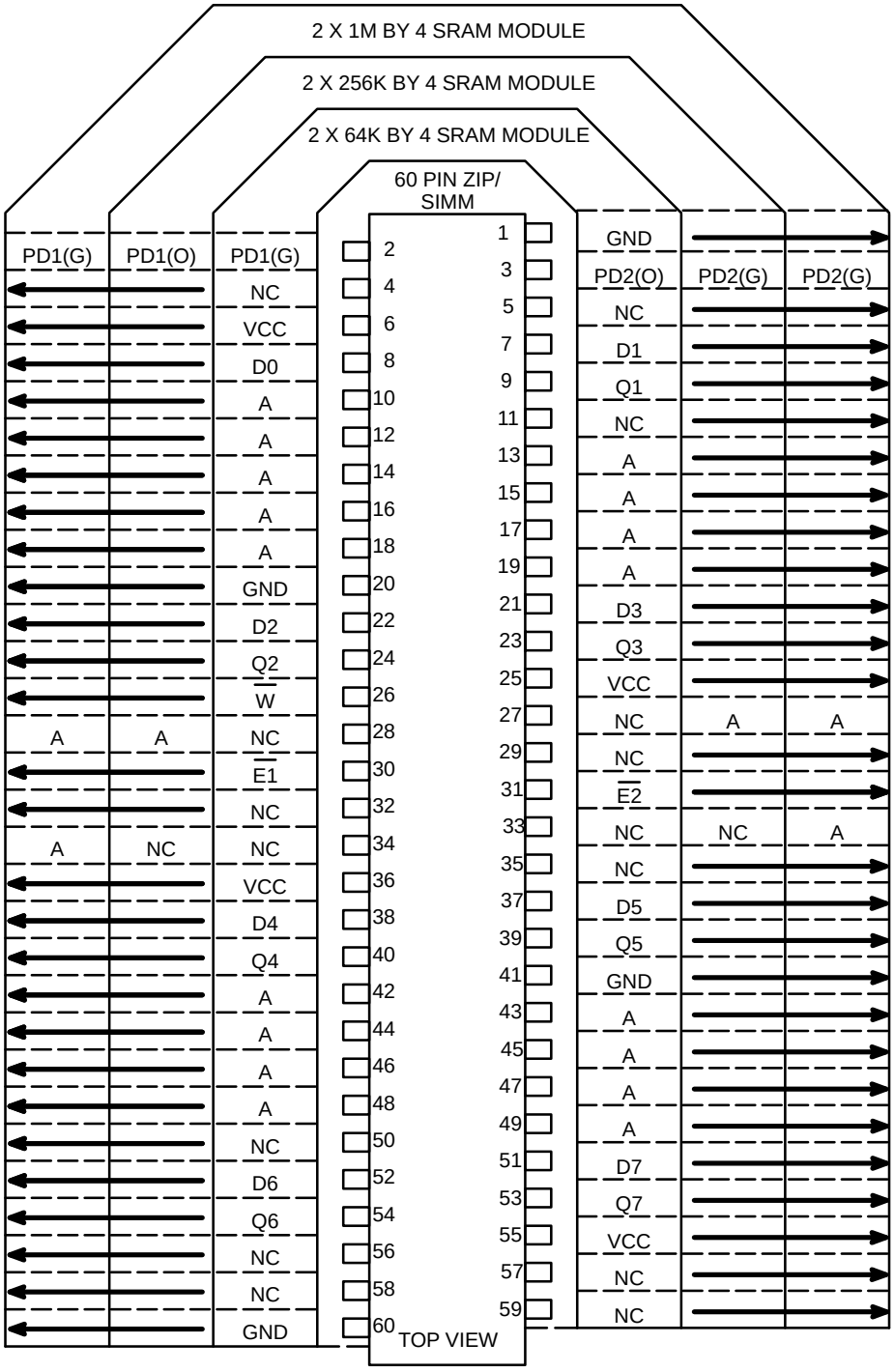
& THIS CONFIGURATION IS APPLICABLE TO 256K, 1M, & 4M X 4 DEVICES.

% THIS CONFIGURATION IS APPLICABLE TO A 16M X 4 DEVICE

* THESE ADDRESS PINS ARE NC WHEN NOT NEEDED FOR THE MEMORY DEVICE USED.

FIGURE 4.2–3

23/25/26/28 PIN DRAM MODULE FAMILY

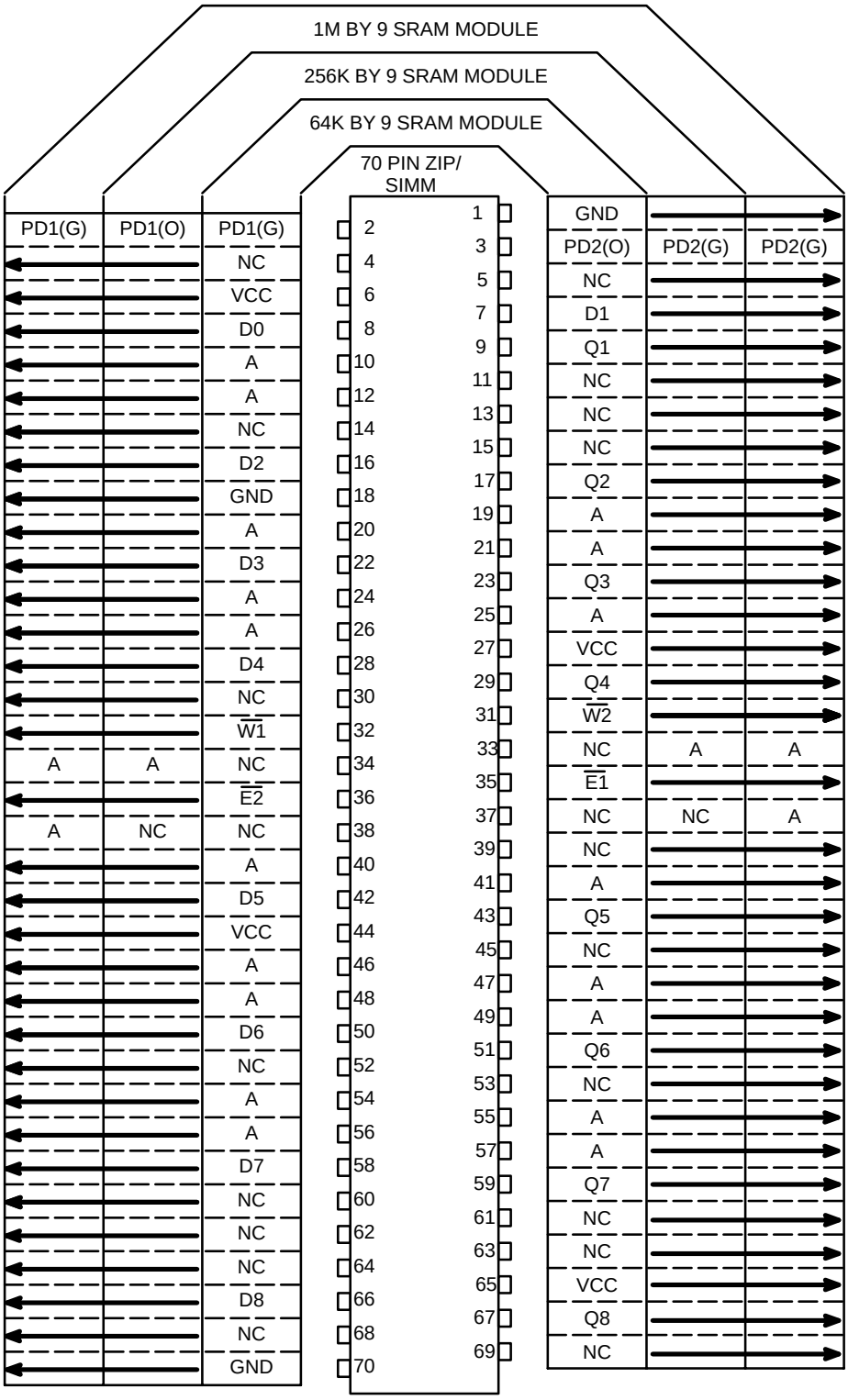


The PD(n) pins are connected to GND (G) or left optn (O).

E1 ENABLES Q0, Q2, Q4, & Q6
E2 ENABLES Q1, Q3, Q5, & Q7

FIGURE 4.2–4

2 X 64K TO 1M BY 4, 60 PIN SRAM MODULE FAMILY



The PD(n) pins are connected to GND (G) or left optn (O).

E1 & W1 CONTROL Q0, Q1, Q2, Q3, Q5, Q6, Q7, Q8
E2 & W2 CONTROL Q4

FIGURE 4.2–5

64K TO 1M BY 9, 70 PIN SRAM MODULE FAMILY